

Appl. No. 10/007,543
Amdt. dated 12/6/05
Reply to Office Action of 11/15/05

PATENT
Docket: 010396

IN THE CLAIMS

1. Cancel.
2. (Previously Amended) A CDMA demodulator, comprising:
a finger timing unit for generating signals indicating cycle boundaries for a plurality of fingers;
an offline processing unit for receiving and storing samples and processing symbols from the stored samples for the plurality of fingers in response to the cycle boundary signals; and
a digital signal processor (DSP) for symbol demodulating and combining the processed symbols corresponding to the plurality of fingers.
3. (Presently Amended) A CDMA demodulator, comprising:
a finger timing unit for generating signals indicating cycle boundaries for a plurality of fingers;
an offline processing unit for receiving and storing samples and processing symbols from the stored samples for the plurality of fingers in response to the cycle boundary signals; and
an engine for symbol demodulating and combining high rate symbols corresponding to the plurality of fingers.
4. (Presently Amended) A CDMA demodulator, comprising:
a memory for storing samples according to a memory address;
a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom;
a register for storing the memory address in response to a processing cycle boundary signal; and
a sample processor for processing samples from the memory identified in accordance with the stored memory address, the sample processing initiated in response to the cycle

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boundary signal, wherein the finger timing unit comprises a plurality of counters for producing the time reference for each of the plurality of fingers.

5. (Previously Amended) A CDMA demodulator, comprising:
a memory for storing samples according to a memory address;
a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom;
a register for storing the memory address in response to a processing cycle boundary signal; and
a sample processor for processing samples from the memory identified in accordance with the stored memory address, wherein the location of samples in the memory for processing in the sample processor is computed by subtracting the processing cycle length from the stored memory address.

6. (Presently Amended) The demodulator of claim [4] 5, wherein the finger timing unit comprises a plurality of counters for producing the time reference for each of the plurality of fingers.

7. (Previously Amended) A CDMA demodulator, comprising:
a memory for storing samples according to a memory address;
a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom, wherein the finger timing unit comprises a single counter and a plurality of masks for producing the time reference for each of the plurality of fingers;
a register for storing the memory address in response to a processing cycle boundary signal; and
a sample processor for processing samples from the memory identified in accordance with the stored memory address.

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8. (Presently Amended) The demodulator of claim [4] 7, wherein the processing cycle boundary signal is a symbol.

9. (Previously Amended) A CDMA demodulator, comprising:
a memory for storing samples according to a memory address;
a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom;
a register for storing the memory address in response to a processing cycle boundary signal; and
a sample processor for processing samples from the memory identified in accordance with the stored memory address,
wherein the sample processor comprises:
a pseudo-random noise (PN) generator for generating PN values; and
a despreader for despreading the samples with the PN values to produce despread samples.

10. (Original) The demodulator of claim 9, further comprising a register for storing the time reference corresponding to and in response to a processing cycle boundary signal.

11. (Original) The demodulator of claim 10, wherein the PN generator comprises a memory, loaded with the PN sequence values, which is addressed in accordance with the stored time reference.

12. (Original) The demodulator of claim 11, wherein the address is computed by subtracting the processing cycle length from the stored time reference.

13. (Original) The demodulator of claim 11, wherein the address is computed by adding a base station specific offset to the stored time reference and subtracting the processing cycle length from the result thereof.

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14. (Original) The demodulator of claim 9, wherein the sample processor further comprises:

- a Walsh generator for generating Walsh chips; and
- a Walsh decoder for discovering the despread samples to produce discovered samples.

15. (Original) The demodulator of claim 14, wherein the sample processor further comprises an accumulator for accumulating the discovered samples for one or more channels.

16. (Previously Amended) A CDMA demodulator, comprising:
a memory for storing samples according to a memory address;
a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom;
a register for storing the memory address in response to a processing cycle boundary signal;
a sample processor for processing samples from the memory identified in accordance with the stored memory address; and
an interrupt controller for arbitrating between the plurality of processing cycle boundary signals.

17. (Previously Amended) A CDMA demodulator, comprising:
a memory for storing samples according to a memory address;
a finger timing unit for producing a time reference for each of a plurality of fingers and producing a plurality of processing cycle boundary signals therefrom;
a register for storing the memory address in response to a processing cycle boundary signal;
a sample processor for processing samples from the memory identified in accordance with the stored memory address; and
a DSP for processing and combining the results of the sample processor.

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18. (Original) The demodulator of claim 17, further comprising a direct memory access (DMA) controller for delivering the output of the sample processor to the DSP.

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21. Cancel.

22. (Presently Amended) A method of CDMA demodulation, comprising:
storing received I and Q samples in a memory according to a memory address;
producing a time reference for a plurality of fingers;
generating interrupts on processing cycle boundaries according to the plurality of time
references;
processing stored samples using an offline processing unit;
~~The method of claim 21, further comprising:~~
latching the memory address upon generating an interrupt; and
accessing the stored samples for processing using an address generated from the latched memory address.

23. (Presently Amended) A method of CDMA demodulation, comprising:
storing received I and Q samples in a memory according to a memory address;
producing a time reference for a plurality of fingers;
generating interrupts on processing cycle boundaries according to the plurality of time
references;
processing stored samples using an offline processing unit; and
~~—The method of claim 21, further comprising:~~
arbitrating between simultaneous assertions of interrupts corresponding to one or more of the plurality of time references.

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24. (Presently Amended) A method of CDMA demodulation, comprising:
storing received I and Q samples in a memory according to a memory address;
producing a time reference for a plurality of fingers;
generating interrupts on processing cycle boundaries according to the plurality of time
references;
processing stored samples using an offline processing unit; and
~~_____The method of claim 21, further comprising:~~
symbol demodulation and combining of the results of the offline processing unit
in a DSP.

25. (Original) The method of claim 24, further comprising:
performing time tracking for the plurality of time references in the DSP; and
updating the plurality of time references in accordance with the time tracking.

26. (Original) The method of claim 24, further comprising:
performing power control decoding in the DSP; and
modifying transmit power in accordance with the power control decoding.--